CLAIMS

What is claimed is:

1. A process for manufacturing an integrated circuit package comprising:

mounting a semiconductor die, to a first surface of a substrate such that bumps on said semiconductor die are electrically connected to conductive traces of said substrate;

mounting at least one collapsible spacer to at least one of a heat spreader, said semiconductor die and said substrate;

fixing said heat spreader to at least one of said first surface of said substrate and said semiconductor die such that said at least one collapsible spacer is disposed therebetween;

forming a ball grid array on a second surface of said substrate, bumps of said ball grid array being electrically connected to said conductive traces; and

singulating said integrated circuit package.

2. The process for manufacturing an integrated circuit package according to claim 1, wherein fixing said heat spreader comprises:

placing one of said heat spreader and said substrate in a mold cavity;

releasably clamping the other of said heat spreader and said substrate to a die of said mold cavity, such that said collapsible spacer is disposed between said heat spreader and said substrate; and

molding a molding compound in the mold, thereby molding the semiconductor die, the substrate, said at least one collapsible spacer and said heat spreader into the molding compound to provide a molded package.

3. The process for manufacturing an integrated circuit package according to claim 1, wherein fixing said heat spreader comprises thermal curing of the at least one collapsible spacer.

4. The process for manufacturing an integrated circuit package according to claim 1, wherein fixing said heat spreader comprises reflowing of the at least one collapsible spacer.

5. The process according to claim 1, wherein said mounting a semiconductor die comprises mounting said semiconductor die in a flip-chip orientation, to said substrate.

6. The process according to claim 5, wherein said mounting said mounting said semiconductor die comprises solder reflowing thereby connecting said bumps of said semiconductor die in said flip-chip orientation to said conductive traces of said substrate.

7. The process according to claim 5, wherein said mounting further comprises underfilling said semiconductor die.

8. The process according to claim 2, wherein said placing one of said heat spreader and said substrate in a mold cavity comprises placing said heat spreader in said mold cavity such that said heat spreader rests on a lower die of said mold and said releasably clamping comprises releasably clamping said substrate to an upper die of said mold.

9. The process according to claim 2, wherein said placing one of said heat spreader and said substrate in a mold cavity comprises placing said substrate in said mold cavity such that said substrate rests on a lower die of said mold and said releasably clamping comprises releasably clamping said heat spreader to an upper die of said mold.

10. The process according to claim 1, wherein said mounting at least one collapsible spacer comprises mounting said at least one collapsible spacer to said substrate.

11. The process according to claim 1, wherein said mounting at least one collapsible spacer comprises mounting said at least one collapsible spacer to said heat spreader.

12. The process according to claim 1, wherein said at least one collapsible spacer comprises a plurality of collapsible spacers, and mounting said at least one collapsible spacer comprises mounting one of said plurality of collapsible spacers to said semiconductor die and mounting at least another of said collapsible spacers to said substrate.

13. The process according to claim 12, wherein said one of said plurality of collapsible spacers is disposed between and in contact with said heat spreader during molding.

14. The process according to claim 13, wherein said at least another of said collapsible spacers is disposed in contact with said heat spreader during molding.

15. A process for manufacturing a plurality of integrated circuit packages comprising:

mounting a plurality of semiconductor dice to a first surface of a substrate array such that bumps on said semiconductor dice are electrically connected to conductive traces of said substrate;

mounting a collapsible spacer array to one of a heat spreader array and said substrate array;

placing one of said heat spreader array and said substrate array in a mold cavity;

releasably clamping the other of said heat spreader array and said substrate array to a first die of said mold such that said collapsible spacer array is disposed between said heat spreader array and said substrate array;

molding a molding compound in the mold, thereby molding the semiconductor dice, said substrate array, said collapsible spacer array and said heat spreader array into the molding compound to provide an array of molded packages;

forming a plurality of ball grid arrays on a second surface of said substrate array, bumps of said ball grid arrays being electrically connected to said conductive traces; and

singulating each integrated circuit package from said array of molded packages.

16. The process according to claim 15, wherein said mounting said plurality of semiconductor dice comprises mounting said semiconductor dice in a flip-chip orientation, to said substrate array.

17. The process according to claim 16, wherein said mounting said plurality of semiconductor dice comprises solder reflowing thereby connecting said bumps of said semiconductor dice in said flip-chip orientation to said conductive traces of said substrate array.

18. The process according to claim 16, wherein said mounting said plurality of semiconductor dice further comprises underfilling said semiconductor dice.

19. The process according to claim 15, wherein said placing one of said heat spreader array and said substrate array in a mold cavity comprises placing said heat spreader array in said mold cavity such that said heat spreader array rests on a lower die of said mold and said releasably clamping comprises releasably clamping said substrate array to an upper die of said

mold.

20. The process according to claim 15, wherein said placing one of said heat spreader array and said substrate array in a mold cavity comprises placing said substrate array in said mold cavity such that said substrate array rests on a lower die of said mold and said releasably clamping, comprises releasably clamping said heat spreader array to an upper die of said mold.

21. The process according to claim 15, wherein said mounting said collapsible spacer array comprises mounting said collapsible spacer array to said substrate array.

22. The process according to claim 15, wherein said mounting said collapsible spacer array comprises mounting said collapsible spacer array to said heat spreader array.

23. The process according to claim 21, wherein mounting said collapsible spacer array further comprises mounting a corresponding collapsible spacer of said collapsible spacer array to each of said plurality of semiconductor dice.

24. The process according to claim 23, wherein said collapsible spacer array is disposed between and in contact with said heat spreader during molding.

25. An integrated circuit package comprising:

a substrate having a plurality of conductive traces;

a semiconductor die flip-chip mounted to a first surface of said substrate, bumps of said semiconductor die being electrically connected to said ones of said plurality of conductive traces;

a heat spreader disposed proximal to and spaced from said semiconductor die by at least one collapsible spacer; and

a ball grid array on a second surface of said substrate, bumps of said ball grid array being electrically connected to said conductive traces.

26. The integrated circuit package according to claim 25, further comprising an underfill material disposed between said semiconductor die and said substrate;

27. The integrated circuit package according to claim 25, wherein said at least one collapsible spacer comprises a collapsible spacer disposed between and in contact with said heat spreader and said semiconductor die.

28. The integrated circuit package according to claim 26, wherein said at least one collapsible spacer further comprises a plurality of collapsible spacers disposed between and in contact with said heat spreader and said substrate array.

29. The integrated circuit package according to claim 25, further comprising a molding compound encapsulating the semiconductor die and said collapsible spacer between the substrate and the heat spreader.

30. An integrated circuit package manufactured by the process according to claim 1.